ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 8, August 2015

Design of Digital Phase Locked Loop for Wireless Communication Receiver Application

Pradnya H.Golghate[1], Prof.Pankaj Hedaoo[2]

Research Scholar[1]

Assistant professor[2]

Abstract: In this paper, Frequency modulated receiver is designed using Digital phase locked loop circuitry which consists of Booth s multiplier, Loop filter and Numerically controlled oscillator. This design is modelled in Verilog synthesis and performed place and route for design using Xilinx 13.1.In this paper, we propose a numerically controlled oscillator that can be tuned to desirable frequency according to the requirement. This design also achieves small area and small power consumption as compared to typical classical method of design.

Index Terms: Digital phase locked loop, Booths multiplier, Numerically Controlled Oscillator.

I. INTRODUCTION

Frequency modulation (FM) is one of the angle modulation techniques. This modulation technique is so common nowadays that it can be found in any kind of commercial radios. The Frequency Modulation (FM) is a method of modifying frequency of carrier signal in order that the receiver can obtain the desired transmitted information. Frequency modulation with sufficient bandwidth provides an advantage in cancelling naturally-occurring noise. This Project uses FM receiver using Digital Phase Locked Circuitry and FIR Filter.

A phase Locked Loop is Electronic circuit which controllers numerically controlled oscillator so that it maintains a constant phase angle relative to the reference signal [2]. In, communication oscillator is at the receiver end and the reference signal is extracted from the signal received from the remote transmitter. Phase locked loop are widely used in space communication for coherent signal tracking, threshold extension, bit synchronisation and symbol synchronisation.

The Digital PLL (DPLL) is really just an Analogy PLL with a digital phase detector. The DPLL is really a hybrid system. The DPLL is very popular in synthesizer application. Digital filters are rapidly replacing classic analog filters .For high-bandwidth signal processing purposes[5]. Frequency

Modulated Receiver circuit in this project uses Digital Phase Locked Loop (DPLL) using Hardware Description Language (HDL) as the main core. This project can also be implemented on FPGA[1]. The design is done using Behavioural Modelling style and Bottom Up methodology. Once the small modules are designed they are integrated using structural methodology. This design has various systems on chip (soc) applications [6]. This paper is organized as follows. Section II describes design of Digital Phase Locked Loop Circuitry. Section III describes Booth's algorithm such as Radix 4 recoding and loop filter design. Section IV describes the numerically controlled oscillator.

Finally results are displayed in Section V and conclusion is presented in Section VI.

II. DESIGN OF DIGITAL PHASE LOCKED LOOP CIRCUITRY

The Digital phase locked loop (DPLL) circuitry mainly consists of Multiplier, Loop Filter and Numerically controlled oscillator. The Design of DPLL circuitry is done using Verilog HDL and simulation is done on Xilinx 13.1.The design can also be implemented using FPGA for further use.

The main task of DPLL is to maintain coherence between (modulated) signal frequency and output frequency by continuous phase comparison. This Self correcting ability of the circuit allows DPLL to track frequency of the output signal once it is tracked. Frequency Modulated input signal is considered as a series of 8 bit digital data.

A. A. Phase Detector:

Phase detector is also known as multiplier module [7].This project uses Booth's Multiplier, as Detector module that will detect the phase error between the input signal and output signal from Numerically Controlled Oscillator.

B. Loop Filter:

The main task of the loop filter is to remove high frequency components.

C. Numerically Controlled Oscillator:

The numerically controlled oscillator will take the corrective error voltage, and then shifts its output frequency and thus keep the PLL in lock [10]. The figure shows Basic Block Diagram of DPLL circuitry:-

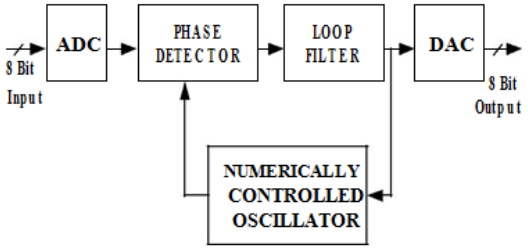


Fig.1. Block Diagram of DPLL Circuitry

DOI 10.17148/IJARCCE.2015.4879

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 8, August 2015

III. BOOTHS ALGORITHM

The Multiplier module also known as Booth s Multiplier is designed using Booths Algorithm. Booth algorithm is an efficient means of multiplying signed numbers expressed in 2's complement notation. It is a powerful algorithm for signed-number multiplication, which operates on both positive and negative numbers uniformly. The Multiplier can receive 8 bit signed number operands A & B, in a register RA and RB, and output the result in 16 bit register Z. At the start of each multiplication cycle, the operands (A & B) are loaded parallel in the registers RA and RB . Each multiplication starts with a LOAD signal and ends with an END signal.

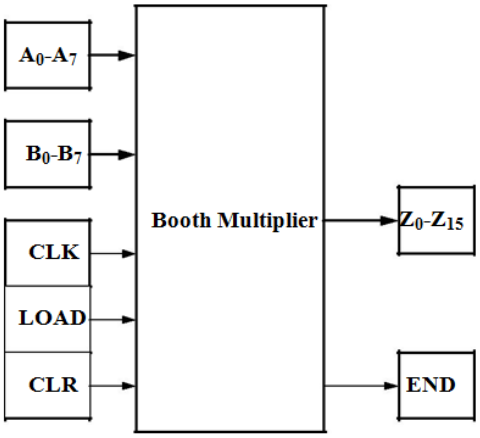


Fig. 2 Schematic Booths Multiplier

A. Radix 4 Booth Recoding:-

Table 1 is used to convert a binary number to Radix-4 number. Initially, a "0" is placed to the right most bit of the multiplier. According to the following equation 3 bits of multiplier are recoded. Table 1 below maps the equation in details.-

Z= X(i+1)+Xi+X(i-1)

Xi+1	Xi	Xi-1	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	2
1	0	0	-2
1	0	1	-1
1	1	0	-1
1	1	1	0

Table.1. Radix-4 Booth Recoding

0	0	0	0*multiplicand
0	0	1	1*multiplicand
0	1	0	1*multiplicand
0	1	1	2*multiplicand
1	0	0	-2*multiplicand
1	0	1	-1*multiplicand
1	1	0	-1*multiplicand
1	1	1	0*multiplicand

Table.2. Multiplier Recoding

In this way Radix-4 Booth s Multiplier is designed using HDL.

B. Loop Filter Design:-

The main task of loop filter is to high frequency components of the system. The input to loop filter is obtained from Phase detector. The input to loop filter is of 16 bits From Booths multiplier. The high frequency elimination is done by bit shifting. This Bit Shifting can be easily obtained by Padding OF Zeros.

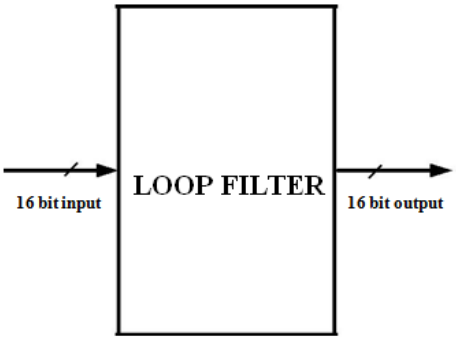


Fig.3 Schematic Loop Filter

IV. NUMERICALLY CONTROLLED OSCILLATOR

This Project uses Numerically Controlled Oscillator NCO) instead of Voltage Controlled Oscillator. The task of NCO is to take corrective input voltage (digital signal) from Loop Filter and then shift its output frequency and in this manner keeping the PPL circuitry always locked.

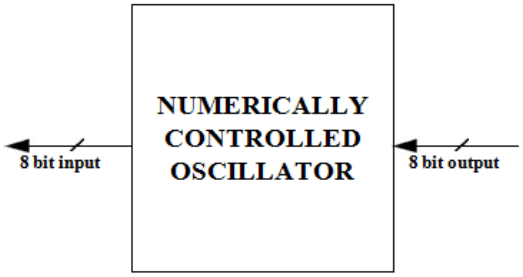
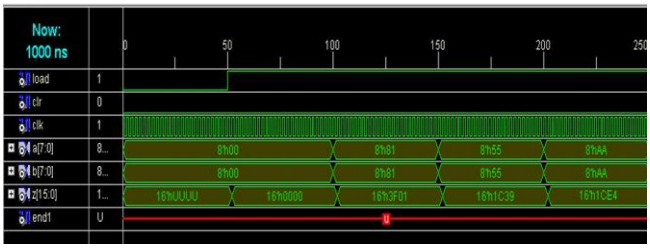


Fig.4 Schematic of NCO

V.RESULT

In this paper, Digital Phase Locked Loop circuitry used in FM Receiver is modelled in Virology using Xilinx ISE 13.l. The design was targeted on the Xilinx Virtex-5 device. The Simulation results Obtained for Digital PLL are shown below:-

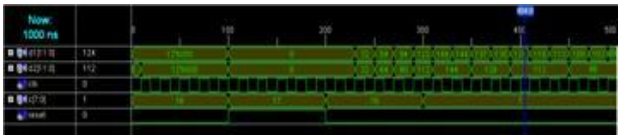
1. 2.Phase Detector Simulation Result:-



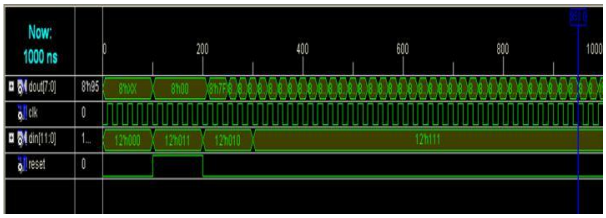
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 8, August 2015

2. Loop Filter Simulation:-



3. Numerically Controlled Oscillator Simulation:-



VI. CONCLUSION

In This Paper, Digital PLL Circuitry is designed using Virology HDL and simulation of results are shown above.

VII. EXPERIMENTAL RESULTS

Module	Parameter	Previous Reported Design	Proposed Design
Booth Multiplier	LUT S	200	165
	Max.Freq	81.38MHz	197.55MHz
	Slices	108	96
Loop Filter	LUT S	52	24
	Max.Freq	320.25MHz	352.40MHz
	Slices	48	24
Numerically Controlled Oscillator	LUT S	275	159
	Max.Freq	165.51MHz	113.59MHz
	Slices	152	50

REFERENCES

[1] Yu-Qing Bao and Yang Li, "FPGA-Based Design of Grid Friendly Appliance Controller,"IEEE TRANSACTIONS ON SMART GRID VOL .5, NO.2, MARCH 2014.

[2] Chao-Wen Tzeng, Shi-Yu Huang, "Parameterized All-Digital PLL Architecture and its Compiler to Support Easy Process Migration"IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL.22, NO.3, MARCH 2014

[3] Wei Deng Ahmed Musa, Teerachot Siriburanon , Masaya Miyahara , Kenichi Okada and Akira Matsuzawa, "A Dual-loop Injection-locked PLL with ALL-digital Background Calibration System for On-chip Clock Generation",2014 IEEE.

[4] Ba You Jie Wang Songyang Li, " FPGA-Based Induction heating with Variable Modulus Control All-Digital Phase-Locked Loop Research"2013 2nd International Conference on Measurement, Information and Control.

[5] C.-C. Chung and C.-Y. Lee, "An all-digital phase-locked loop for high speed Clock generation," IEEE J. Solid-State Circuits, vol. 38, no. 2, pp. 347–351, Feb. 2003.

[6] T. Olsson and P. Nilsson, "A digitally controlled PLL for SoC applications," IEEE J. Solid-State Circuits, vol. 39, no. 5, pp. 751–760, May 2004.

[7] M. Combs, K. Dioury, and A. Greiner, "A portable clock multiplier Generator using digital CMOS standard cells," IEEE J. Solid-State Circuits, vol. 31, no. 7, pp. 958–965, Jul. 1996

[8] P. M. Anderson and M. Mirheydar, "A low-order system frequency response model," IEEE Trans. Power Syst., vol. 5, no. 3, pp. 720–729, 1990.

[9] D. Sheng, C.-C. Chung, and C.-Y. Lee, "An all-digital phase-locked loop With high-resolution for SoC applications," in Proc. Int. Symp. VLSI Design Autom. Test, Apr. 2006, pp. 1–4.

[10] P.-L. Chen,C.-C.Chung, and C.-Y. Lee, "A portable digitally controlled Oscillator using novel varactors," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 5, pp. 233–2